Circuit f r pr grammable stepless cl ck shifting

Technical Field

The present invention relates to a circuit for programmable stepless clock shifting.

This application is based on, and claims the benefit of, European Patent Application No. 03290424.5 filed on February 21, 2003 which is incorporated by reference herein.

Background of the Invention

In many electronic applications, for example digital CDRs (Clock Recovery Unit), it is required to generate a clock signal with a programmable phase shift with respect to a reference clock.

In a number of situations, when transferring data between different chips, boards or devices, the associated clock is usually not distributed. The main reason is pin count reduction and power saving. At the receiving end, the problem of recovering the associated clock arises, in order to sample and process the incoming data stream. The operation of phase aligning often cannot be avoided also when the associated clock signal is distributed along with the data signal.

It is possible to design a clock recovery circuit working without a reference clock under precise assumptions on the data pattern and the local VCO frequency tuning range. Since these hypothesis is often not met in the applications, the known solutions mainly require a reference clock frequency within a well defined tolerated range.

A number of known techniques are already available for generating a clock signal with a programmable phase shift, namely delay locked loops (DLL), phase locked loops (PLL), open loop delay lines, digital phase aligners (DPA).

PLL based solutions require considerable power and chip area and are generally not able to cope with a wide range data transition density or long CID

(continuous identical digits) sequences, as often required by applications.

Often a PLL is used to generate N phases of the reference clock. They are all distributed to each receiving macro in which one is selected in order to sample the incoming data. This solution requires a lot of area for the wiring. Besides, switching noise, variations in phase difference between the clock multiphases and duty cycle distortion become a challenging issue when covering a long path; in addition the mimimum distance in degrees between two adiacent phases is limited by the technology used for the chip.

In other proposed schemes, one PLL is used to generate one filtered clock phase which is then distributed to all the receiving macros. Locally all the phases are generated by means of a DLL. Power consumption and occupation area remain a severe issue. Also in these cases the mimimum distance in degrees between two adiacent phases is limited by the technology.

Cases in which the multi-phase clock is generated by means of an open loop delay line are also known. In this schemes, power consumption (all the phases are generated also if not used) is an issue. Moreover the whole algorithm is complicated because the phases do not cover 360° and the phase spacing is PTV (process, temperature and supply) dependent and limited.

Solutions that delay the data (digital phase aligners, DPA) are also known. The main drawback is that the delay chain length is supposed to cover the jitter tolerance amplitude and not only the clock period, which results in longer delay chains. This implies more eye closure and again a PTV dependent and limited phase spacing. Moreover, an architecture that delays the data requires the local availability of the exact transmitter clock frequency.

Summary of the Invention

Therefore in view of the known solutions, that are not quite efficient, it is the main object of the present invention to provide a circuit for programmable stepless clock shifting solving all the above mentioned problems.

The basic idea of the present invention is to provide a programmable stepless clock shifter, consisting of a splitter generating a 0° and a 90° shifted clocks from a reference clock, and an interpolator of this two phases, which

provides at the output the desired pre-set clock phase.

This object is achieved by a circuit for programmable stepless clock shifting comprising:

- a splitter, receiving a clock reference and generating two 90°-shifted clock phases;
- an interpolator receiving said two 90°-shifted clock phases and two coefficients, and supplying a programmable phase clock, which has a phase shift with respect to said clock reference that depends only on said two coefficients.

Brief Description of the Drawings

The invention will become fully clear from the following detailed description, given by way of a mere exemplifying and non limiting example, to be read with reference to the attached drawing, wherein the single figure shows a block diagram of the circuit in accordance with the invention.

Best Mode for Carrying Out the Invention

As shown in the figure, the solution consists of two blocks in series, a splitter (SPLITTER) and an interpolator (INTERPOLATOR): the splitter receives a clock CK_REF and generates two clock phases, 90° shifted; the interpolator uses these two clock phases and two coefficients SIN_Φ and COS_Φ, and produces a clock, which has a phase that depends only on the input coefficients.

A detailed description of the two blocks is given in the following.

SPLITTER. The input clock CK_REF is summed (in the adder S1) and substracted (in the subtractor S2) to a delayed clock CK_DEL supplied by a delaying circuit DEL. It is possible to show analitically or graphically that the two clocks at the outputs of S1 and S2 are 90° shifted for construction, independently on the value of delay Δ as soon as the following condition on the delay is met:

$\Delta \neq \pi + k\pi$, k ={0, ±1, ±2, ...}

This means that the vectorial product of the input clock CK_REF and the delayed clock CK_DEL should not be zero. In the applications this condition is easily met.

Typically the value of Δ is 90° ± 50%.

When the input clock CK_REF and the delayed clock CK_DEL are orthogonal, that means shifted exactly by 90° each other, the output amplitudes of S1 and S2 are equal. In the other cases two squarers SQ1 and SQ2 are encharged to output two clocks CK_90 and CK_0 with the same amplitude. In practice in the circuit implementation the two squarers are ever present to ensure output amplitude uniformity.

INTERPOLATOR. This block receives the two 90° shifted clocks CK_90 and CK_0 from the splitter and provides a clock with a phase that is programmable by setting two appropriate input coefficients.

The working principle relies on the following trigonometric relation:

$\sin(\omega t+\Phi) = \sin(\omega t)\cos\Phi + \cos(\omega t)\sin\Phi$

By summing two 90° shifted clock phases, $\sin(\omega t)$ and $\cos(\omega t)$, with appropriate coefficients, $\cos\Phi$ and $\sin\Phi$, it is possible to obtain any delayed version $\sin(\omega t+\Phi)$, of the input reference clock $\sin(\omega t)$.

In the circuit the two 90° shifted clocks CK_90 and CK_0 are sent to respective inputs of two multipliers M1 and M2; the second input of M1 is supplied with a first coefficient SIN_Φ and the second input of M2 with a second coefficient COS_Φ.

The outputs of M1 and M2 are supplied to the inputs of an adder S3 wich gives at the output the wanted clock reference CK_REF_Φ with the pre-set phase difference Φ with respect to the input clock CK_REF.

The two coefficients SIN_Φ and COS_Φ are selected in any wanted way. For example they can come from a memory table TAB suitably addressed, according to the wanted phase shift Φ, which can be any.

The advantages of the present invention are clear.

The minimum angle between two adiacent phases is not technology nor temperature nor supply dependent. The resolution can be chosen as high as needed (stepless clock shifter).

The solution is open loop, so it does not require a careful design of the loop in order to grant stability. When used in CDRs, no minimum data transition density has to be defined.

A monolitic chip implementation, for example a VLSI technology, takes advantage of the low power consumption and the low silicon area required. No filter has to be implemented.

Further implementation details will not be described, as the man skilled in the art is able to carry out the invention starting from the teaching of the above description.

Many changes, modifications, variations and other uses and applications of the subject invention will become apparent to those skilled in the art after considering the specification and the accompanying drawings which disclose preferred embodiments thereof. All such changes, modifications, variations and other uses and applications which do not depart from the spirit and scope of the invention are deemed to be covered by this invention.